What Is Claimed Is:

1. A semiconductor device having a semiconductor chip formed with a transistor,

wherein said transistor has a first electrode, a second electrode, and a control electrode,

wherein each of said first and second electrodes is constructed by a base portion and a plurality of fingers projected in a direction orthogonal to said base portion,

wherein one of the fingers of said first electrode is disposed between neighboring two fingers of said second electrode,

wherein said second electrode is connected to a fixed potential, and

wherein a width of each of said fingers positioned at both ends of said second electrode is wider than a width of each of said fingers positioned between said both ends.

2. The semiconductor device according to claim 1, wherein the width of each of said fingers positioned at both ends is equal to or wider than a sum of the widths of said plurality of fingers positioned between said both ends.

3. The semiconductor device according to claim 1, wherein the width of said base portion of said second electrode is wider than the width of each of said fingers

positioned at both ends.

4. The semiconductor device according to claim 1, wherein said first electrode is a drain electrode, said second electrode is a source electrode, and said control electrode is a gate electrode.

5. The semiconductor device according to claim 1, wherein said first electrode is a collector electrode, said second electrode is an emitter electrode, and said control electrode is a base electrode.

6. The semiconductor device according to claim 1, wherein said base portions of said electrodes extend in the same direction, and said fingers of said electrodes extend in a direction orthogonal to an extending direction of said base portions.

7. A power amplifier device having one or a plurality of amplification systems,

wherein said amplification system has a semiconductor chip in which a transistor is formed and a plurality of external electrode terminals,

wherein said external electrode terminals are an input terminal to which a signal to be amplified is supplied, an output terminal for outputting the amplified signal, and first, second, and third power source terminals,

wherein said transistor is electrically connected between said input terminal and said output terminal,

wherein electrodes of said transistor are a control electrode connected to said input terminal and said third power source terminal, a first electrode connected to said output terminal and said first power source terminal, and a second electrode connected to said second power source terminal serving as an earth terminal,

wherein over a top face of said semiconductor chip, an electrode pad corresponding to said external electrode terminal and a plurality of electrode pads formed in a portion of said second electrode of said transistor are provided,

wherein a conductive wire for electrically connecting said external electrode terminal with said electrode pad corresponding to the external electrode terminal, and a conductive wire for electrically connecting the plurality of electrode pads formed in the portion of said second electrode of said transistor with said second power source terminal are provided,

wherein each of said electrodes of said transistor is constructed by a base portion and a plurality of fingers projected in a direction orthogonal to said base portion, one of the fingers of said first electrode is disposed between two neighboring fingers of said second electrode,

wherein said second electrode is connected to a fixed potential, and

wherein a width of each of said fingers positioned at both ends of said second electrode is wider than a width of each of said fingers positioned between said both ends.

8. The power amplifier device according to claim 7, wherein the width of each of said fingers positioned at both ends is equal to or wider than a sum of the widths of said plurality of fingers positioned between said both ends.

9. The power amplifier device according to claim 7, wherein the width of said base portion of said second electrode is wider than the width of each of said fingers positioned at both ends.

10. The power amplifier device according to claim 7, wherein said first electrode is a drain electrode, said second electrode is a source electrode, and said control electrode is a gate electrode.

11. The power amplifier device according to claim 7, wherein said first electrode is a collector electrode, said second electrode is an emitter electrode, and said control electrode is a base electrode.

12. The power amplifier device according to claim

7, wherein two transistors are formed in said semiconductor chip and are electrically connected in parallel with each other between said input terminal and said output terminal.

13. The power amplifier device according to claim 7, further comprising:

a supporting substrate mounting said semiconductor chip and constructing said second power source terminal;

a plurality of leads disposed around said supporting substrate and constructing said external electrode terminals; and

a sealing part made of an insulating resin for covering said supporting substrate, said external electrode terminal, said semiconductor chip, and said wire in a state where an under face and an external end face of each of said supporting substrate and said external electrode terminal are exposed.

14. The power amplifier device according to claim 13, wherein said sealing part has a square shape in plan view, and an external end face of said external electrode terminal is flush with a peripheral face of said sealing part.

15. The power amplifier device according to claim 7, wherein a plurality of transistors are cascaded between

said input terminal and said output terminal to thereby obtaining a multi-stage amplification configuration.

16. The power amplifier device according to claim 7, wherein said base portions of said electrodes of said transistor extend in the same direction, said fingers of said electrodes extend in a direction orthogonal to an extending direction of each of said base portions, and each of said fingers extends in a direction orthogonal to a line connecting said input terminal with said output terminal.

17. The power amplifier device according to claim 7, wherein said power amplifier device is a power amplifier device for a wireless LAN of a 5-GHz band.

18. A personal computer card having a power amplifier device for transmission connected to an antenna, wherein said power amplifier device has the configuration of claim 7.

19. The personal computer card according to claim 18, comprising:

a transmission/reception change-over switch connected to said antenna;

a low-noise amplifier for reception connected to said transmission/reception change-over switch;

a reception-system mixer connected to said low-noise amplifier for reception;

a base band LSI connected to said reception-system mixer;

a transmission-system mixer connected to said base band LSI; and

a voltage controlled oscillator connected to said base band LSI, said reception-system mixer, and said transmission-system mixer,

wherein said power amplifier device for transmission is connected to said transmission-system mixer and said transmission/reception change-over switch.